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ATTORNEY'S DOCKET NO: S1022.80385US00

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patentee:	Antonino Torres and Sergio Tommaso Spampinato	
Serial No.:	09/497,916	Patent No. 6,815,779 B1
Filed:	February 4, 2000	Issued: November 9, 2004
For:	AN INTEGRATED CIRCUIT INCLUDING PROTECTION AGAINST POLARITY INVERSION OF THE SUBSTRATE POTENTIAL	

Examiner:	Ori Nadav		
Art Unit:	2811	Confirmation No.:	8061

ATTN: Certificate of Correction Branch
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir/Madam:

Transmitted herewith for filing is/are the following document(s):

[X] Request for Certificate of Correction
[X] Copies of: Listing of the Claims from 06/28/04 Amend; Page 1 of Apl as Filed; and Cols 1 and 8 of U.S. 6,815,779
[X] PTO Form SB/44
[X] Return Post Card

If the enclosed papers are considered incomplete, the Mail Room and/or the Application Branch is respectfully requested to contact the undersigned collect at (617)720-3500, Boston, Massachusetts.

No check is enclosed. If it is determined that a fee is necessary, the fee may be charged to the account of the undersigned, Deposit Account No. 23/2825. A duplicate of this sheet is enclosed.

CERTIFICATE OF MAILING UNDER 37 C.F.R. §1.8(a)

I hereby certify that this document is being placed in the United States mail with first-class postage attached, addressed to Correspondence and Mail Division, Certificate of Correction Branch, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the 18th day of November, 2004.

Attorney Docket No.: S1022.80385US00
XNDD

Respectfully submitted,

Antonino Torres et al., Patentee

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patentee:	Antonino Torres and Sergio Tommaso Spampinato		
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P.O. Box 1450
Alexandria, VA 22313-1450

REQUEST FOR CERTIFICATE
OF CORRECTION UNDER 37 C.F.R. §1.322

Sir/Madam:

Patentees respectfully request the correction of an error in the above-captioned patent. Specifically, there is a spelling error in the Field of the Invention section and text has been omitted from claim 20 of issued U.S. Patent No. 6,815,779.

The first paragraph of U.S. Patent No. 6,815,779 reads:

> The present invention relates to the field of **intergrated** circuits. More specifically, the invention relates to a structure for the protection of integrated circuits against polarity inversion of the substrate potential. (Emphasis added)

However, as originally filed on February 4, 2000 the first paragraph read:

> The present invention relates to the field of **integrated** circuits. More specifically, the invention relates to a structure for the protection of integrated circuits against polarity inversion of the substrate potential. (Emphasis added)

The word "integrated" was not misspelled at the time this application was filed, nor was any amendment made, by either Patentees or the Examiner at any time during prosecution, to the

specification making this change. Therefore it is respectfully requested that a Certificate of Correction be granted to correct this error.

Claim 20 of U.S. Patent No. 6,815,779 reads:

20. A semiconductor device, comprising:
(A) a vertical power component having a terminal formed by a substrate of a first conductivity type;
(B) a control circuit, isolated from the substrate by an isolation region of a second conductivity type; and
(C) a protection structure against polarity inversion of a substrate potential, comprising:
(i) a first bipolar transistor having an emitter connected to said isolation region and a collector connected to a reference potential input of the integrated circuit;
(ii) a bias circuit that biases the first bipolar transistor in a reverse saturation mode when the substrate is at a potential higher than a reference potential; and
(iii) means for coupling the isolation region to the substrate through a high impedance when the substrate potential is lower than the reference potential,
the first bipolar transistor is directly connected to the isolation region.

In the last Listing of the Claims which was submitted to the Patent Office in the Amendment filed on June 28, 2004 claim 20 read as shown below:

20. A semiconductor device, comprising:
(A) a vertical power component having a terminal formed by a substrate of a first conductivity type;
(B) a control circuit, isolated from the substrate by an isolation region of a second conductivity type; and
(C) a protection structure against polarity inversion of a substrate potential, comprising:
(i) a first bipolar transistor having an emitter connected to said isolation region and a collector connected to a reference potential input of the integrated circuit;
(ii) a bias circuit that biases the first bipolar transistor in a reverse saturation mode when the substrate is at a potential higher than a reference potential; and
(iii) means for coupling the isolation region to the substrate through a high impedance when the substrate potential is lower than the reference potential,
wherein the emitter of the first bipolar transistor is directly connected to the isolation region. (Emphasis added)

The words "wherein the emitter of" were part of claim 20 as shown in the Listing of the Claims. No further amendment was made by Patentees or the Examiner after June 28, 2004 deleting this text.

In support of this Request, Patentees submit herewith a highlighted Listing of the Claims from the amendment filed on June 28, 2004, page 1 of the application as filed on February 4, 2000 and columns 1 and 8 of U.S. 6,815,779

Patentees request that a Certificate of Correction be granted in U.S. Letters Patent No. 6,815,779 as specified herein and on the attached Certificate of Correction form SB/44.

The corrections requested do not involve change in the patent that constitutes new matter or would require reexamination. Therefore, it is respectfully requested that the corrections be made and that a Certificate of Correction be issued.

Patentees respectfully submit that, since the errors for which a Certificate of Correction is sought was the result of Patent Office mistake, no fee is due. However, if the Examiner deems a fee necessary, the fee may be charged to the account of the undersigned, Deposit Account No. 23/2825.

Should any questions arise concerning the foregoing, please contact the undersigned at the telephone number listed below.

CERTIFICATE OF MAILING UNDER 37 C.F.R. §1.8(a)

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DEC 03 2004

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AN INTEGRATED CIRCUIT INCLUDING A VERTICAL POWER COMPONENT, A CONTROL CIRCUITRY THEREOF, AND A PROTECTION STRUCTURE AGAINST POLARITY INVERSION OF THE SUBSTRATE POTENTIAL

Background Of The Invention

1. Field of the Invention

The present invention relates to the field of integrated circuits. More specifically, the invention relates to a structure for the protection of integrated circuits against polarity inversion of the substrate potential.

2. Discussion of the Related Art

VIPower ("Vertical Intelligent Power) denotes integrated circuits which, in a same chip, integrate one or more vertical power components (power bipolar transistors) and a circuitry (control circuitry) for controlling the switching of the power components.

VIPower integrated circuits typically comprise a common semiconductor substrate forming one electrode of the power component.

In VIPower integrated circuits, in order to electrically separate from each other and from the substrate the components of the control circuitry, a P type doped region (called an isolation region) is provided.

Figure 1 shows in cross-section a portion of a control circuitry of a VIPower integrated circuit. On an N+ substrate 1, an N- layer 2 is epitaxially formed. A P type isolation region 3 is formed inside the N- layer 2. The P type isolation region 3 defines two isolated N- layer portions 4, 5 which are isolated from each other and from the N- layer 2. Inside N- layer portion 4 a PNP bipolar transistor T1 of the control circuitry is formed, while in the N- layer portion 5 an NPN bipolar transistor T2 of the control circuitry is formed.

By properly biasing the P type isolation region 3 at the ground potential (or, more generally, at the lowest potential existing in the integrated circuit), the PN junctions formed by the isolation region 3, the N- layer 2 and the N- layer portions 4, 5 are reverse-biased, so that electrical isolation is achieved. This is necessary in order to assure that parasitic bipolar transistors Qn1, Qn2, Qn3 are kept off.

In VIPower technology, the PN junction formed by the P type isolation region 3 and the N- layer 2 has a structure capable of sustaining high reverse voltages, typically of

In The Claims

Applicants submit below a complete listing of the current claims, with insertions indicated by underlining and deletions indicated by strikeouts and/or double bracketing.

Listing of the Claims

1. (Currently Amended) An integrated circuit including a vertical power component having a terminal formed by a chip substrate of a first conductivity type, a control circuit thereof, the control circuit isolated from the substrate by means of an isolation region of a second conductivity type, and a protection structure against polarity inversion of a substrate potential comprising a first bipolar transistor with an emitter connected to said isolation region and a collector connected to a reference potential input of the integrated circuit, the reference potential input providing a reference potential, a bias circuit for biasing the first bipolar transistor in a reverse saturated mode when the substrate potential is higher than the reference potential, and a second bipolar transistor with an emitter connected to the substrate and a base coupled to the isolation region for coupling the isolation region to the substrate through a high-impedance when the substrate potential is lower than the reference potential and the first bipolar transistor is off.

2. (Original) An integrated circuit according to claim 1, wherein said bias circuit comprises a third bipolar transistor with an emitter coupled to control terminal of the integrated circuit and a collector coupled to a base of the first bipolar transistor, said control terminal receiving an external control signal which is used by the control circuit to cause switching of the power component, said control signal being used to provide a voltage supply to the control circuit and to the bias circuit.

3. (Previously Presented) An integrated circuit according to claim 2, wherein said first bipolar transistor is a vertical transistor having an emitter formed by said substrate, a collector formed by a second doped region of the first conductivity type, and a base formed by a first doped region of the second conductivity type formed in the substrate and within the first doped region.

4. (Previously Presented) An integrated circuit according to claim 3, wherein said first and third bipolar transistors are isolated from the substrate by said isolation region.

5. (Original) An integrated circuit according to claim 4, wherein said first conductivity type is the N type, said second conductivity type is the P type, said first and second bipolar transistors are NPN transistors, and said third bipolar transistor is a PNP transistor.

6. (Original) An integrated circuit according to claim 1, wherein said vertical power component is a vertical power bipolar transistor.

7. (Currently Amended) A semiconductor device, comprising:

(A) a vertical power component having a terminal formed by a substrate of a first conductivity type;

(B) a control circuit, isolated from the substrate by an isolation region of a second conductivity type; and

(C) a protection structure against polarity inversion of a substrate potential, comprising:

(i) a first bipolar transistor having an emitter connected to said isolation region and a collector connected to a reference potential input of the integrated circuit, the reference potential input providing a reference potential;

(ii) a bias circuit that biases the first bipolar transistor in a reverse saturation mode when the substrate is at a potential higher than ~~a~~ the reference potential; and

(iii) means for coupling the isolation region to the substrate through a high impedance when the substrate potential is lower than the reference potential and the first bipolar transistor is off.

8. (Previously Presented) The device of claim 7, wherein the second bipolar transistor forms a regulation loop that reduces parasitic transistor action from affecting the first bipolar transistor and the bias circuit.

9. (Previously Presented) The device of claim 7, wherein the vertical power component comprises a vertical power bipolar transistor.

10. (Previously Presented) The integrated circuit of claim 1, wherein the first bipolar transistor couples the isolation region to the reference potential input when the substrate potential is higher than the reference potential.

11. (Previously Presented) The integrated circuit of claim 1, wherein the first bipolar transistor is off when the substrate potential is less than the reference potential.

12. (Previously Presented) The integrated circuit of claim 1, wherein the emitter of the first bipolar transistor is directly connected to the isolation region.

13. (Previously Presented) The integrated circuit of claim 1, wherein the collector of the first bipolar transistor is directly connected to the reference potential input.

14. (Previously Presented) The integrated circuit of claim 1, wherein the emitter of the second bipolar transistor is directly connected to the substrate.

15. (Previously Presented) The semiconductor device of claim 7, wherein the first bipolar transistor couples the isolation region to the reference potential input when the substrate potential is higher than the reference potential.

16. (Previously Presented) The semiconductor device of claim 7, wherein the first bipolar transistor is off when the substrate potential is less than the reference potential.

17. (Previously Presented) The semiconductor device of claim 7, wherein the emitter of the first bipolar transistor is directly connected to the isolation region.

18. (Previously Presented) The semiconductor device of claim 7, wherein the collector of the first bipolar transistor is directly connected to the reference potential input.

19. (Previously Presented) An integrated circuit including a vertical power component having a terminal formed by a chip substrate of a first conductivity type, a control circuit thereof, the control circuit isolated from the substrate by means of an isolation region of a second conductivity type, and a protection structure against polarity inversion of a substrate potential comprising a first bipolar transistor with an emitter connected to said isolation region and a collector connected to a reference potential input of the integrated circuit, a bias circuit for biasing the first bipolar transistor in a reverse saturated mode when the substrate potential is higher than the reference potential, and a second bipolar transistor with an emitter connected to the substrate and a base coupled to the isolation region for coupling the isolation region to the substrate through a high-impedance when the substrate potential is lower than the reference potential, and

wherein the emitter of the first bipolar transistor is directly connected to the isolation region.

20. (Previously Presented) A semiconductor device, comprising:

(A) a vertical power component having a terminal formed by a substrate of a first conductivity type;

(B) a control circuit, isolated from the substrate by an isolation region of a second conductivity type; and

(C) a protection structure against polarity inversion of a substrate potential, comprising:

(i) a first bipolar transistor having an emitter connected to said isolation region and a collector connected to a reference potential input of the integrated circuit;

(ii) a bias circuit that biases the first bipolar transistor in a reverse saturation mode when the substrate is at a potential higher than a reference potential; and

(iii) means for coupling the isolation region to the substrate through a high impedance when the substrate potential is lower than the reference potential,

wherein the emitter of the first bipolar transistor is directly connected to the isolation region.

INTEGRATED CIRCUIT INCLUDING PROTECTION AGAINST POLARITY INVERSION OF THE SUBSTRATE POTENTIAL

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to the field of intergrated circuits. More specifically, the invention relates to a structure for the protection of integrated circuits against polarity inversion of the substrate potential.

2. Discussion of the Related Art

VIPower ("Vertical Intelligent Power) denotes integrated circuits which, in a same chip, integrate one or more vertical power components (power bipolar transistors) and a circuitry (control circuitry) for controlling the switching of the power components.

VIPower integrated circuits typically comprise a common semiconductor substrate forming one electrode of the power component.

In VIPower integrated circuits, in order to electrically separate from each other and from the substrate the components of the control circuitry, a P type doped region (called an isolation region) is provided.

FIG. **1** shows in cross-section a portion of a control circuitry of a VIPower integrated circuit. On an N+ substrate **1**, an N– layer **2** is epitaxially formed. A P type isolation region **3** is formed inside the N– layer **2**. The P type isolation region **3** defines two isolated N– layer portions **4**, **5** which are isolated from each other and from the N– layer **2**. Inside N– layer portion **4** a PNP bipolar transistor T1 of the control circuitry is formed, while in the N– layer portion **5** an NPN bipolar transistor T2 of the control circuitry is formed.

By properly biasing the P type isolation region **3** at the ground potential (or, more generally, at the lowest potential existing in the integrated circuit), the PN junctions formed by the isolation region **3**, the N– layer **2** and the N– layer portions **4**, **5** are reverse-biased, so that electrical isolation is achieved. This is necessary in order to assure that parasitic bipolar transistors Qn1, Qn2, Qn3 are kept off.

In VIPower technology, the PN junction formed by the P type isolation region **3** and the N– layer **2** has a structure capable of sustaining high reverse voltages, typically of some hundreds of volts.

FIG. **2** is a schematic electrical diagram showing a possible use of a VIPower integrated circuit. Specifically, FIG. **2** depicts a circuit arrangement wherein a VIPower integrated circuit **8** is used for controlling a high-voltage IGBT (Insulated Gate Bipolar Transistor) **7**. The VIPower integrated circuit chip **8** and the IGBT chip **7** are advantageously housed in a same package **6** and constitute a driver for a coil **9**. In this arrangement the common N+ substrate of the VIPower integrated circuit **8** (N+ substrate **1** in FIG. **1**) is electrically connected to the collector of the IGBT **7**. In the example shown in FIG. **2**, wherein an IGBT is used, the IGBT chip and the VIPower chip are advantageously housed in a same package. This is only an example. If the power device used to drive the coil were a power bipolar transistor, which can be directly integrated in the VIPower chip, the VIPower chip can directly drive the coil, without the need of having an IGBT chip.

Externally, the package **6** appears as a three-terminal device having a control terminal **10** (receiving a control or trigger signal TRIGGER, typically a logic signal switching between ground and 5 V) and two drive terminals **11**, **12**. Terminal **12** is connected to a first battery pole, providing a reference potential (ground). Terminal **11** is connected to a first terminal of the coil **9**, the second terminal of the coil **9** being connected to a second battery pole BAT which, in normal operating conditions, is at a potential higher than that of the first pole.

Referring to the circuit arrangement of FIG. **2**, it is necessary to guarantee that in case the polarity of the battery is inadvertently inverted the VIPower integrated circuit is not destroyed. Typical battery voltages have values up to 24 V. So, the VIPower integrated circuit must be capable of sustaining reverse voltages of –24 V without being damaged.

The IGBT inherently has a structure capable of sustaining such reverse voltages. By contrast, as far as the control circuitry is concerned, if the P type isolation region **3** is kept biased at the ground voltage as usual, and if the polarity of the battery were inadvertently inverted, the PN junction between the P type isolation region and the substrate would be forward biased, which would cause the destruction of the VIPower integrated circuit.

The same problem is encountered even if the IGBT is not provided, and the power component (power bipolar transistor) directly integrated in the VIPower chip is used to directly drive the coil.

It is thus necessary to properly bias the P type isolation region, so as to assure that not only the components of the control circuitry are electrically isolated from each other and from the substrate, but also the possibility of an inversion of the polarity of the substrate potential.

A known solution is described in U.S. Pat. No. 5,382,837. FIG. **3** is an electrical equivalent circuit of such a solution. FIG. **4** is a circuit diagram similar to that of FIG. **3**, showing a possible practical implementation of the circuit of FIG. **3**. With reference to FIG. **3**, the isolation region (ISO) of the control circuitry of the VIPower integrated circuit is connected to the common collectors of two NPN bipolar transistors Q1, Q2. Transistor Q1 has the emitter connected to ground, transistor Q2 has the emitter connected to the substrate (SUB) of the VIPower integrated circuit. The base of transistor Q1 is connected through a bias resistor R1 to a voltage supply Vd. The base of transistor Q2 is kept at a constant pre-set bias voltage by a bias circuit **13**, a possible implementation of which is shown in FIG. **4**. All the transistors that are connected to the substrate of the VIPower integrated circuit, such as Q2 in FIGS. **3** and **4**, are high-voltage vertical transistors whose emitter coincides with the substrate and whose base is a P type doped region similar to but isolated from the P type isolation region of the control circuitry of the VIPower integrated circuit.

In the circuits of FIGS. **3** and **4**, in normal operating conditions, when the potential of the substrate (SUB) is positive, transistor Q2 is off and transistor Q1, in saturation, biases the isolation region (ISO) at VCE,sat(Q1). If the substrate potential goes negative, transistor Q2, whose base current is supplied by transistor Q3 (FIG. **4**), goes into saturation, so that the isolation region ISO is biased at a voltage equal to the negative potential of the substrate plus VCE,sat(Q2).

The drawback of the circuits shown in FIGS. **3** and **4** is that they require a supply voltage Vd for their operation. On the contrary, in the arrangement of FIG. **2**, the control signal TRIGGER which determines the coil charge time, is also used as a supply voltage for the control circuitry of the VIPower integrated circuit. Signal TRIGGER is not acti-

ity type is the P type, said first and second bipolar transistors are NPN transistors, and said third bipolar transistor is a PNP transistor.

6. An integrated circuit according to claim **1**, wherein said vertical power component is a vertical power bipolar transistor.

7. The integrated circuit of claim **1**, wherein the first bipolar transistor couples the isolation region to the reference potential input when the substrate potential is higher than the reference potential.

8. The integrated circuit of claim **1**, wherein the first bipolar transistor is off when the substrate potential is less than the reference potential.

9. The integrated circuit of claim **1**, wherein the emitter of the first bipolar transistor is directly connected to the isolation region.

10. The integrated circuit of claim **1**, wherein the collector of the first bipolar transistor is directly connected to the reference potential input.

11. The integrated circuit of claim **1**, wherein the emitter of the second bipolar transistor is directly connected to the substrate.

12. A semiconductor device, comprising:

(A) a vertical power component having a terminal formed by a substrate of a first conductivity type;

(B) a control circuit, isolated from the substrate by an isolation region of a second conductivity type; and

(C) a protection structure against polarity inversion of a substrate potential, comprising:

(i) a first bipolar transistor having an emitter connected to said isolation region and a collector connected to a reference potential input of the integrated circuit, the reference potential input providing a reference potential;

(ii) a bias circuit that biases the first bipolar transistor in a reverse saturation mode when the substrate is at a potential higher than the reference potential; and

(iii) means for coupling the isolation region to the substrate through a high impedance when the substrate potential is lower than the reference potential and the first bipolar transistor is off.

13. The device of claim **12**, wherein the second bipolar transistor forms a regulation loop that reduces parasitic transistor action from affecting the first bipolar transistor and the bias circuit.

14. The device of claim **12**, wherein the vertical power component comprises a vertical power bipolar transistor.

15. The semiconductor device of claim **12**, wherein the first bipolar transistor couples the isolation region to the reference potential input when the substrate potential is higher than the reference potential.

16. The semiconductor device of claim **12**, wherein the first bipolar transistor is off when the substrate potential is less than the reference potential.

17. The semiconductor device of claim **12**, wherein the emitter of the first bipolar transistor is directly connected to the isolation region.

18. The semiconductor device of claim **12**, wherein the collector of the first bipolar transistor is directly connected to the reference potential input.

19. An integrated circuit including a vertical power component having a terminal formed by a chip substrate of a first conductivity type, a control circuit thereof, the control circuit isolated from the substrate by means of an isolation region of a second conductivity type, and a protection structure against polarity inversion of a substrate potential comprising a first bipolar transistor with an emitter connected to said isolation region and a collector connected to a reference potential input of the integrated circuit, a bias circuit for biasing the first bipolar transistor in a reverse saturated mode when the substrate potential is higher than the reference potential, and a second bipolar transistor with an emitter connected to the substrate and a base coupled to the isolation region for coupling the isolation region to the substrate through a high-impedance when the substrate potential is lower than the reference potential, and

wherein the emitter of the first bipolar transistor is directly connected to the isolation region.

20. A semiconductor device, comprising:

(A) a vertical power component having a terminal formed by a substrate of a first conductivity type;

(B) a control circuit, isolated from the substrate by an isolation region of a second conductivity type; and

(C) a protection structure against polarity inversion of a substrate potential, comprising:

(i) a first bipolar transistor having an emitter connected to said isolation region and a collector connected to a reference potential input of the integrated circuit;

(ii) a bias circuit that biases the first bipolar transistor in a reverse saturation mode when the substrate is at a potential higher than a reference potential; and

(iii) means for coupling the isolation region to the substrate through a high impedance when the substrate potential is lower than the reference potential,

the first bipolar transistor is directly connected to the isolation region.

* * * * *

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U.S. Patent and Trademark Office; US. DEPARTMENT OF COMMERCE

(Also Form PTO-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO.	:	6,815,779 B1
DATED	:	November 9, 2004
INVENTOR(S)	:	Antonino Torres Sergio Tommaso Spampinato

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In col. 1, Field on the Invention section, line 9 should read:

--The present invention relates to the field of integrated--

In claim 20, col. 8, line 47 should read

--wherein the emitter of the first bipolar transistor is directly connected to the--

MAILING ADDRESS OF SENDER

PATENT NO. 6,815,779

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DEC 03 2004